

Demonstration of low-power bit-interleaving TDM PON

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Abstract: A functional demonstration of bit-interleaving TDM downstream protocol for passive optical networks (Bi-PON) is reported. The proposed protocol presents a significant reduction in dynamic power consumption in the customer premise equipment over the conventional TDM protocol. It allows to select the relevant bits of all aggregated incoming data immediately after clock and data recovery (CDR) and, hence, allows subsequent hardware to run at much lower user rate. Comparison of experimental results of FPGA-based implementations of Bi-PON and XG-PON shows that more than 30x energy-savings in protocol processing is achievable.

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1. Introduction

As the demand for network equipment keeps growing exponentially, power consumption of network equipment is expected to follow, knowing that the dynamic power consumption of a CMOS circuit is proportional to its operating frequency and switching activity [1]. Recent advances in deep sub-micron CMOS technologies may help alleviate the problem, though at the expense of increased static power due to transistor leakages. Besides thermal management related issues and energy cost, the vastness of present-day networks causes network equipment to leave a considerable ecological footprint on our planet. Therefore, disruptive re-design of network architecture, protocols and hardware are vital to support the growth of traffic demand in a sustainable way [2, 3].

This work focuses on the energy consumption of optical access networks, passive optical networks (PONs) in particular. In a PON, an optical line terminal (OLT) at the central office is connected to a number of optical network terminations (ONTs) at the customer premises, typically 32 to 128, over a shared fiber plant. The total power consumption of a PON is dominated by the ONTs simply because of their volume.

Most PONs deployed today adopt a time-division-multiplexing (TDM) scheme as an access mechanism on the shared medium. TDM-based protocols have been specified by the standard bodies [4, 5]. To cope with the increasing bandwidth demand, these protocols have also evolved with a higher line rate [4, 5]. These “super-charged” protocols, however, suffer from the problem of energy inefficiency which is inherited from their predecessors. As the line rates have increased, this problem has become noticeable.

Although results reported in this paper focus on the ITU-T branch TDM protocol, namely XG-PON, the concept proposed here can easily be generalized to the IEEE PON protocols. The rest of the paper is organized as follows. In the next section, energy efficiency of XG-PON is analyzed. Deficiencies of the protocol from the power consumption perspective are highlighted. The third section describes a newly proposed bit-interleaving TDM protocol, namely Bi-PON [6]. Implementation and performance evaluation of Bi-PON are discussed in the fourth section. Experimental results obtained from prototyping both XG-PON and Bi-PON are compared. Finally, conclusions are presented in the last section.

This paper is an expanded version of our publication at ECOC 2012 [7]. In this paper, the Bi-PON protocol is discussed in more detail and the architecture of the Bi-PON ONT is disclosed to better explain how the protocol facilitates considerable energy savings to be realized. In addition, experimental results with our recently developed bit-interleaving CDR (Bi-CDR) ASIC [8] are compared with XG-PON and an FPGA-based implementation of Bi-PON.

2. Energy deficiencies of XG-PON protocol

Figure 1 shows a simplified block diagram of a XG-PON ONT downstream operation. As described previously, a PON is a shared topology meaning that the information for all receivers is broadcasted and presented to every single receiver. As illustrated in red, the XG-PON protocol is defined such that a series of complex receiver functions must be performed at the receiving line rate, i.e. 10 Gb/s. At the end of this chain, the XG-PON encapsulation method (XGEM) receiver then selects the useful information targeted to the particular ONT. Assuming an average user rate of 100 Mb/s on a PON with 10 Gb/s line rate, 99% of the data processed along this chain is therefore discarded at the XGEM receiver. While operating at a full line rate, the circuits implementing these functions clearly dominate the total power consumption of an ONT. To address this inefficiency, the ITU-T has introduced a cyclic sleep mode mechanism in its recent specification [5]. This sleep mode allows some part of the ONT functions to be turned off (or “sleep”) periodically. However, in order to support this mode, the transmitter will have to accumulate data and deliver it in a batch. The side effects of this mode are that the transmitter

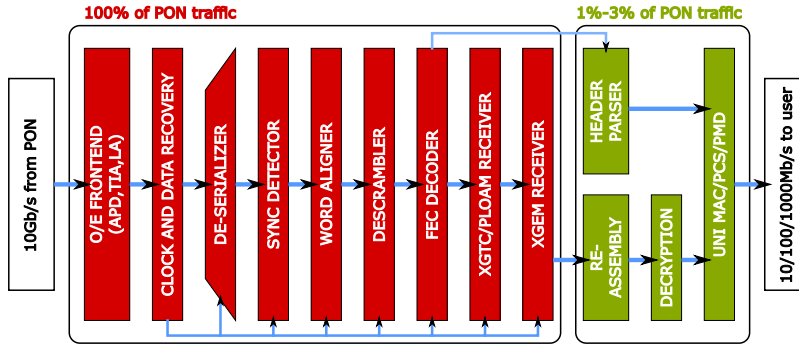


Fig. 1. Downstream architecture of XG-PON ONT

will incur an additional buffering and the quality of service (QoS), specifically, the packet delay and jitter will be greatly affected [10]. Other sleep mode schemes, adaptive link rate (ALR) techniques and combinations of both have been proposed, though all share the mentioned disadvantages [10]. To lower energy consumption, the sleep period will have to be sufficiently long. A long sleep state translates to larger buffering, longer delay and larger delay variation.

This paper only focuses on the downstream protocol because it largely dominates the total power consumption of an ONT. The upstream data path is considered energy efficient given that there is no unrelated traffic being processed. The burst-mode behavior at the upstream transmission is also inherently energy efficient.

3. The bit-interleaving PON protocol (Bi-PON)

To overcome the issue in XG-PON protocol, this paper proposes a Bi-PON protocol which modifies the framing structure of the transmission. Figure 2 explains how the protocol works, different colors are used to denote bits intended for different ONTs. The Bi-PON frame has a fixed length of 125 μ s corresponding to the XG-PON frame. It consists of a header section and a payload section. The header section is further divided into a synchronization field, a bandwidth map field and an operation, administration and maintenance (OAM) field. The main distinguishing feature of the Bi-PON frame is that all information bits residing in all sections are organized in a bit-interleaved fashion according to the targeted ONTs. This scheme contrasts the XG-PON framing where groups of information bits targeted to a particular ONT are placed in various, irregularly spread locations in a frame. Because of this regular structure in a Bi-PON frame, each ONT only needs to extract its own information in a simple periodic fashion.

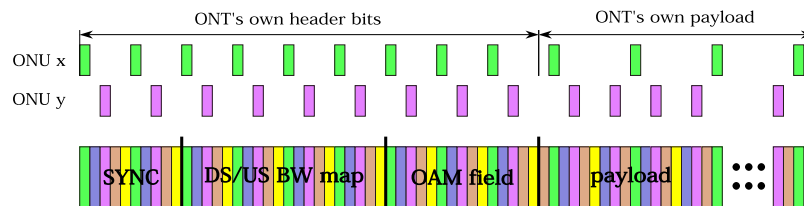


Fig. 2. Bi-PON transmission frame structure

Figure 3 shows a block diagram of the Bi-PON ONT downstream operations. As becomes

clear when comparing Fig. 1 and Fig. 3, the number of functional blocks required to operate at full line rate has been reduced significantly. Immediately after the conversion of the incoming optical signal into the electrical domain by the O/E front-end receiver, the clock and data recovery (CDR) circuit extracts the clocking/timing information and recovers the raw information bits. The Bi-PON protocol supports a fixed number of ONTs, e.g. 256. By matching a synchronization pattern and its own ONT identifier, an ONT only need to “listen” to one of the 256 ONT-channels. The bit-interleaving structure together with the fixed number of ONTs reduces the decimation operation into a simple down-sampler. This contrasts to a more complex de-serialization and word alignment operation found in the XG-PON protocol. And, more importantly, the information rate after the decimator is significantly reduced, from the line rate (i.e., 10 Gb/s) to the user rate, typically below 1 Gb/s as bits intended for other users are immediately discarded. This allows all subsequent operations to be run at a much lower clock rate than the ones in XG-PON. Hence, dynamic power consumption of a Bi-PON ONT is significantly lower.

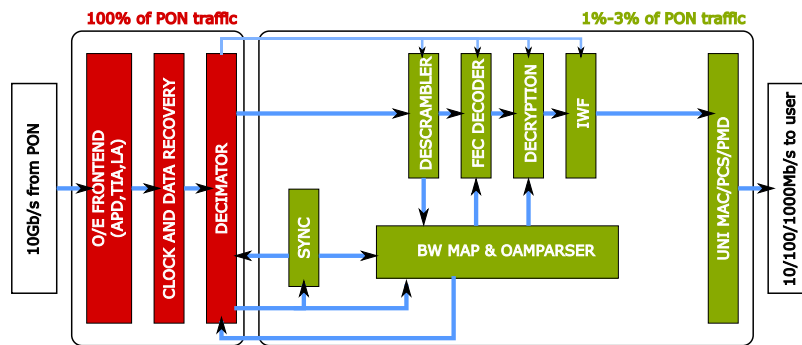


Fig. 3. Downstream architecture of Bi-PON ONT

While the bit allocation scheme in the header section is fixed, the Bi-PON protocol adopts a flexible dynamic bandwidth allocation (DBA) mechanism in the payload section. Within the BW map field, it carries bandwidth allocation information specified as a tuple (S_i, K_i) where K_i is the sampling rate and S_i is the starting offset of an ONT i . Based on this information, the decimator can extract the payload bits that belong to the designated ONT in the payload section. As the OLT composes (S_i, K_i) for all ONTs, it may update this allocation in a frame by frame basis according to the instantaneous traffic profile of the ONTs.

As illustrated in Fig. 2, the protocol also includes an OAM field in the header. The OAM field carries commands such as ranging, encryption keys, etc. A useful OAM command is the “SLEEP CMD” in which the target ONT is instructed to enter a sleep state for the duration of time specified in command argument (in terms of number of frames). During the sleep duration, an ONT shuts off most of the downstream operation except the CDR, decimator and bit-counter to save energy.

4. Processing a Bi-PON frame

The flow-chart in Fig. 4 explains how the ONTs process a BiPON frame. The raw bits are immediately decimated to reduce the working frequency, initially by a factor of e.g. 256. As explained before, the ONT now “listens” to one of 256 channels. The synchronization logic scans this 39 Mb/s bit stream for a synchronization code. The odd and even channels have the same respective synchronization codes, one being the complement of the other to improve on

DC-balancing. Once found, the succeeding channel identifier (ID) code can be read. This ID corresponds to the channel number (0..255) for even channels and its complement for the others, again to achieve DC-balancing. After synchronizing, reading the channel identifier allows offset adjustment of the 256-decimator and, hence, enables the ONT to lock on its proper channel. For following frames, the ONT will again search for the synchronization code and confirm the matching of channel ID to the ONU ID, whereafter the remainder of the header-data would be parsed.

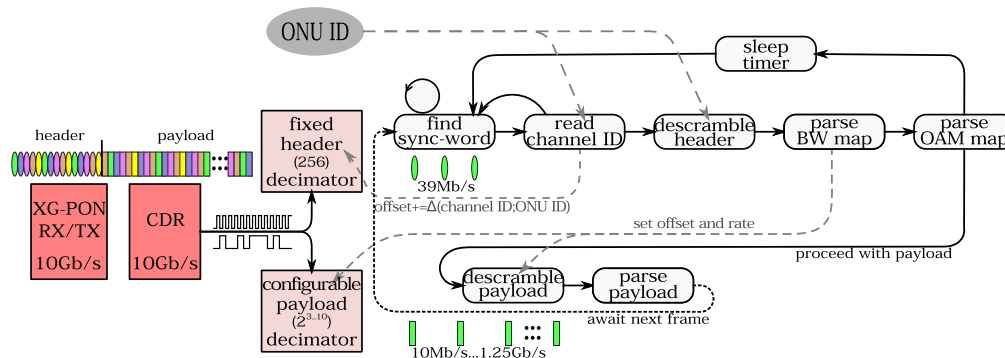


Fig. 4. Flow-chart of Bi-PON frame processing

As an experiment, we have prototyped a basic Bi-PON ONT using an FPGA based design as shown in Fig. 5(a). This design uses an Altera Stratix IV EP4SGX230 device, a 10 Gb/s CDR from Vitesse and off-the-shelf XG-PON transceiver components. For comparison, we have also implemented a basic XG-PON ONT on the same hardware, to allow a fair comparison. Apart from the FEC decoder and decryption modules, the basic ONTs implement all functional modules, as those shown in Fig. 1 and Fig. 3.

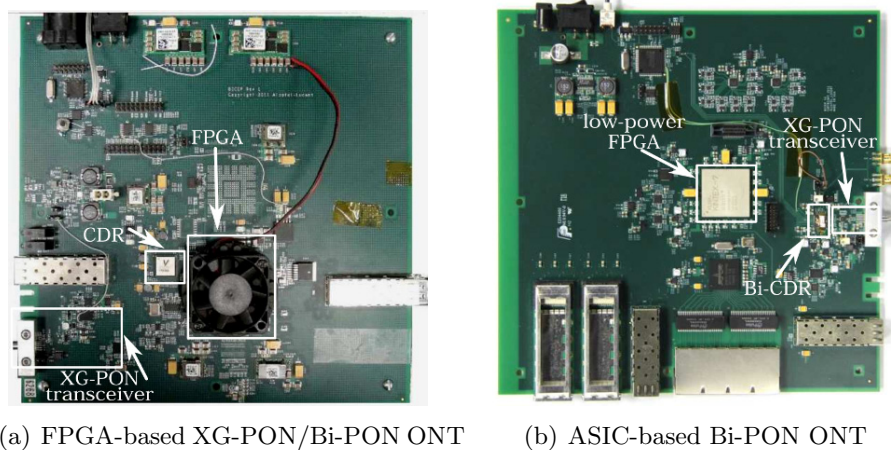


Fig. 5. Experimental prototypes

For the discussion of measurement results, only the downstream path is considered. Comparing the two FPGA-based implementations, the Bi-PON ONT design utilizes significantly less logic and memory resources than the XG-PON ONT design. This is mainly due to the simplified protocol with its ability to greatly reduce the data rate of the incoming data stream to its useful content, very early in the architecture. This reduction in data rate eliminates the requirement of massive parallel data paths and operations. As a result, both dynamic and static power consumption of the Bi-PON ONT are lower than the XG-PON ONT.

As FPGAs are known to have high static power consumption, in order to fairly compare the energy efficiency of two protocols, we have adopted the following methodology to estimate dynamic power consumption. In our experiment, we first measured the power consumption of the board when the input line is removed and all clocks on the board are disabled. This measurement represents a baseline idle (or static) power consumption of the design. Then, we measured the power consumption of a fully operational design at various traffic load conditions. The difference in measured power between a fully operational state and an idle state yields the estimated dynamic power consumption. Dynamic power consumption is a good indicator of the potential savings in the future custom chip design.

Table 1 compares the dynamic power consumption measurements of both FPGA-based designs at different traffic loads, ranging from 1.25Gb/s, over 10Mb/s to “idle” where there is no traffic load (“without sleep” refers to the scenario where there is no bandwidth map, “with sleep” refers to situation where the OAM field signals the ONT to be inactive for a given time and to power down hardware accordingly). It also lists the results of this measurement on the ASIC-based design as reference. The figures for the FPGA-based ONT’s also include the dynamic power consumption of the Vitesse CDR, which is estimated to be about 98 mW. When comparing both FPGA implementations, we notice, as expected, that the ONT implementing the XG-PON protocol suffers from a much higher dynamic power consumption than the one implementing the Bi-PON protocol. At a traffic load of 1.25 Gb/s, a Bi-PON ONT exhibits a $\sim 18\times$ power saving compared to the XG-PON ONT, including the Vitesse CDR. This increases to $\sim 35\times$ when subtracting the power of the CDR. It is also observed that dynamic power consumption of XG-PON does not vary much (or varies within the margin of error in our measurements) at various loading conditions. This is expected since the majority of the op-

erations do not change as the traffic condition varies. For Bi-PON, however, the dynamic power consumption decreases with the reduction of bandwidth allocation. Recall that dynamic power consumption of a CMOS circuit is proportional to its operating frequency. As the operating frequency of functional modules behind the decimator is scaled down, the power consumption is reduced accordingly. At a traffic load of 10 Mb/s, the Bi-PON ONT exhibits a $\sim 180\times$ power saving in protocol processing compared to the XG-PON ONT (without considering the CDR).

As also indicated in Table 1, introducing the sleep mode operation in XG-PON does reduce its power consumption by $\sim 28\%$. However, this reduction is not as significant as one would expect because several key modules in the design cannot be completely shut down without losing their states. In contrast, in a Bi-PON ONT, when there is no BW allocation or when the ONT is in sleep state, most functional modules are inherently shut off as there is no clock or data output from the decimator.

A graph of the dynamic power consumption of both Bi-PON implementations in function of the user data rate is shown in Fig. 6. It is interesting to notice that power dissipation of the Bi-PON ONTs scales well with the user data rate. The static power consumption of the ASIC itself amounts to approximately 130 mW [8]. Migration to a deep sub-micron CMOS technology would allow to further decrease both dynamic and static power consumption as more logic could be implemented in plain CMOS. For the complete test-boards, the static power consumption amounts to 9.5 W for the FPGA-based Bi-PON ONT and 2.9 W for the ASIC-based version.

Table 1. Estimated dynamic power consumption [W]

	XG-PON FPGA	Bi-PON FPGA	Bi-PON ASIC
Active @ 1.25Gb/s	3.7	0.200	NA
Active @ 625Mb/s	3.7	0.163	0.105
Active @ 312Mb/s	3.7	0.142	0.087
Active @ 156Mb/s	3.7	0.135	0.078
Active @ 78Mb/s	3.7	0.127	0.064
Active @ 39Mb/s	3.7	0.122	0.060
Active @ 20Mb/s	3.7	0.120	0.055
Active @ 10Mb/s	3.7	0.118	0.050
Idle without sleep	3.7	0.107	0.050
Idle with sleep	2.7	0.107	0.039

6. Conclusions

This paper discusses energy efficiency of the TDM PON protocols as specified in the current GPON and XG-PON specifications. The requirement to perform computationally intensive – and, hence, power-hungry – operations on all received information before identifying the useful parts hinders highly desired improvements in energy-efficiency. Various sleep modes, adaptive link rate systems and combinations of both have been proposed, though all inherently suffer from limited efficacy and have a negative impact on the link quality. As an alternative, this paper proposes a novel bit-interleaving TDM protocol, which allows to drop most of the bits immediately after clock and data recovery. Additionally, it offers a method for dynamic bandwidth allocation. Results obtained from the functional experiment have demonstrated that a significant saving ($\sim 35\times$ to $\sim 180\times$) in dynamic power consumption can be achieved using the proposed protocol. This astounding saving is achieved by a clever separation and organization

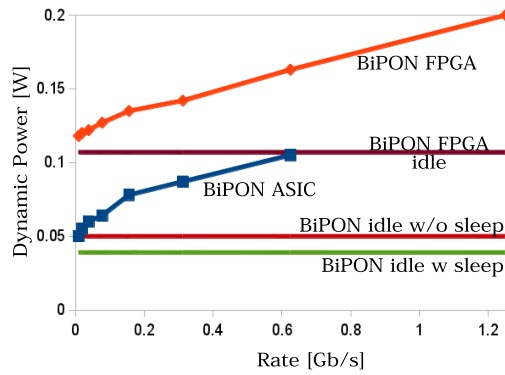


Fig. 6. Strong relationship between dissipation and data rate for Bi-PON

of user information at the physical layer, without sacrificing the flexibility of the PON bandwidth allocation. The energy efficiency of Bi-PON is expected to be even more relevant for the future TDM PON as the downstream line rate grows as high as 40 Gb/s.

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